A graphical comparison of RISC processors

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Abstract

A graphical approach for the comparison of RISC processors is presented in this note. Kiviat graphs summarize some of the most relevant architectural parameters of RISC designs in a more appealing manner as tables of parameters.

1. Introduction

When discussing RISC designs and the difference between RISC and CISC processors, it is often helpful to look at the different architectural parameters in a graphical form. Patterson and Hennessy [1990] include a table of characteristics of some common RISC engines and other authors have conducted similar surveys [Gimarc and Milutinovic 1987]. In this short note we summarize this information, as taken from several sources, and let the pictures speak by themselves. This graphical approach is very appealing for discussions about RISC and CISC processors and has been used with success in the classroom.
We review some of the most important and popular RISC processors. Only the most relevant features of each design are summarized. We have drawn for each processor the corresponding Kiviat graph. This type of graphical representation has been used in other architectural studies [Siewiorek/Bell/Newell 1985, Ferrari et al 1983] and in many fields in which the representation of several dimensions of data must be handled in just two dimensions. We choose for the Kiviat graphs the most relevant parameters for RISC architectures. It is well known that a graphical approach can be superior to numerical tables when several data dimensions are involved [Tufte 1990].
In this note we assume a general knowledge of the RISC design concept as given.

2. The relevant parameters

The variables considered in the comparison of processors are the following:

- number of pipeline stages
- number of addressing modes
- number of instructions
- method of branch handling
- average cycles per instruction (CPI) according to some authors
- number of registers
- instruction length (fixed or variable)
- levels of instruction decoding

The circle shows which points in each axis could be considered as "typical" RISC values: 1) A pipelining depth of four stages, for example, could be considered a normal feature of RISC technology; 2) A single addressing mode is normally associated with a RISC architecture; 3) Several RISC processors use 6 bits for the encoding of instructions: this means that typically only 64 instructions can be encoded; 4) One delayed branch slot could be considered normal in most RISC designs, but there are other alternatives. The IBM RS/6000 for example uses a powerful branch handling method superior in average to delayed branching, but which is also more hardware intensive; 5) The cycles per instruction (CPI) should be ideally one for a RISC engine; 6) Thirty-two registers are typical for most RISC designs; 7) RISC processors have a fixed instruction length; and 8) Hardware decoding of instructions is faster than microprogrammed decoding.
Figures 1 to 6 summarize the architectural parameters of six different RISC processors.

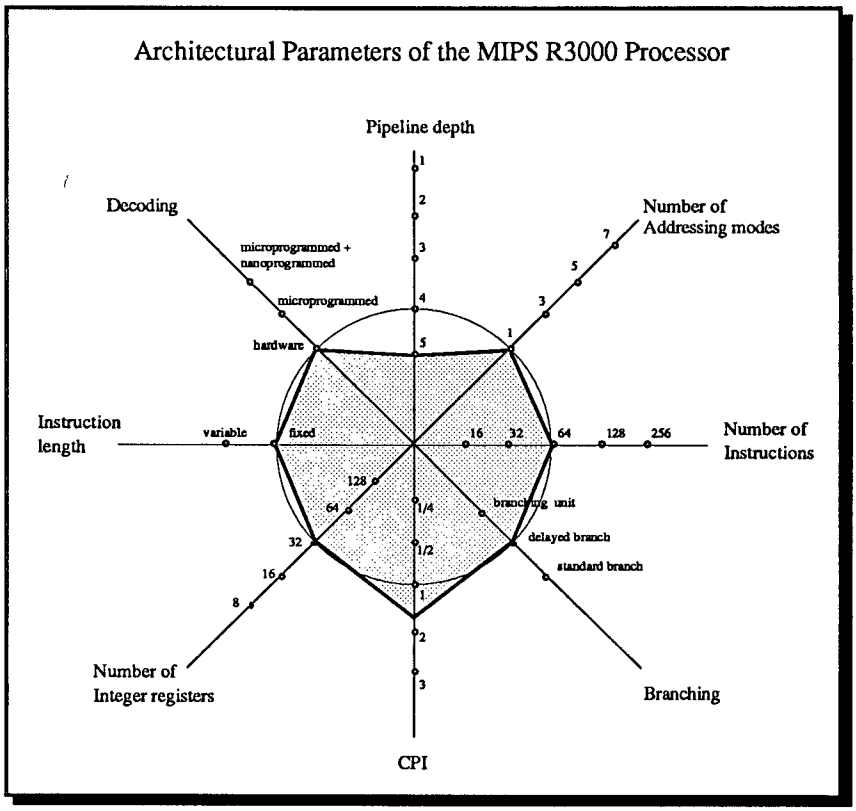

Figure 1

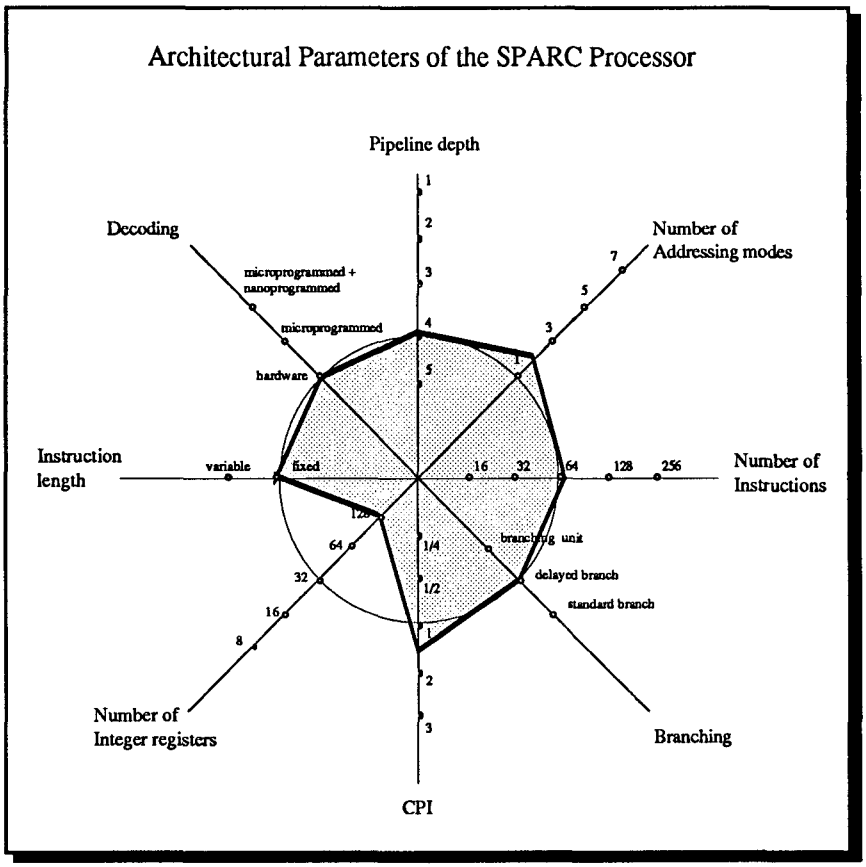

Figure 2

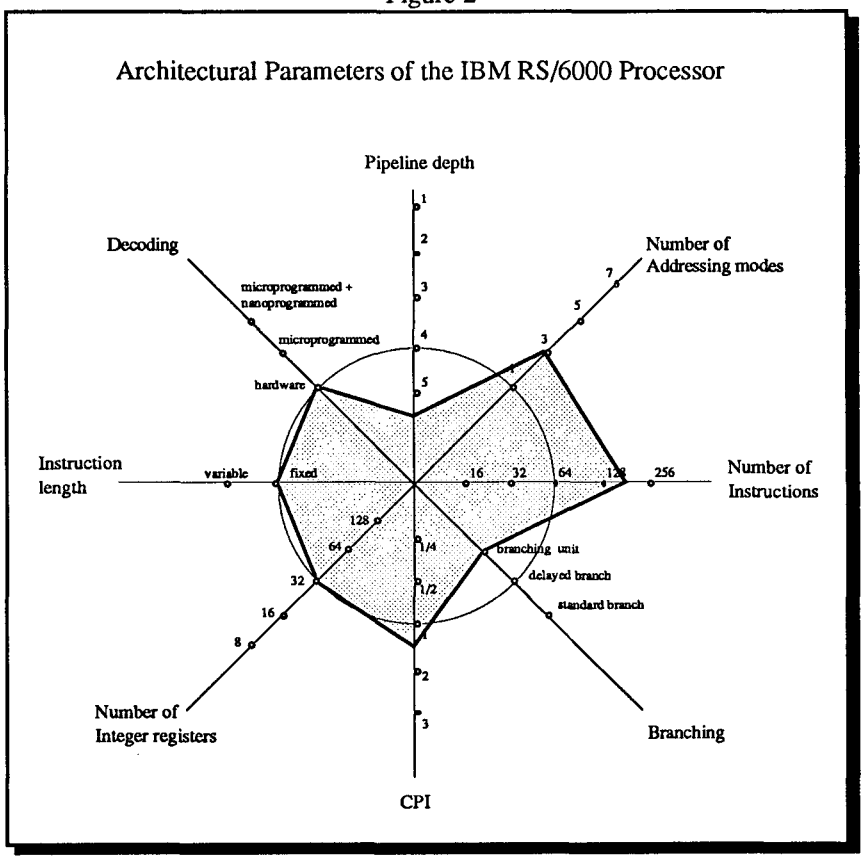

Figure 3

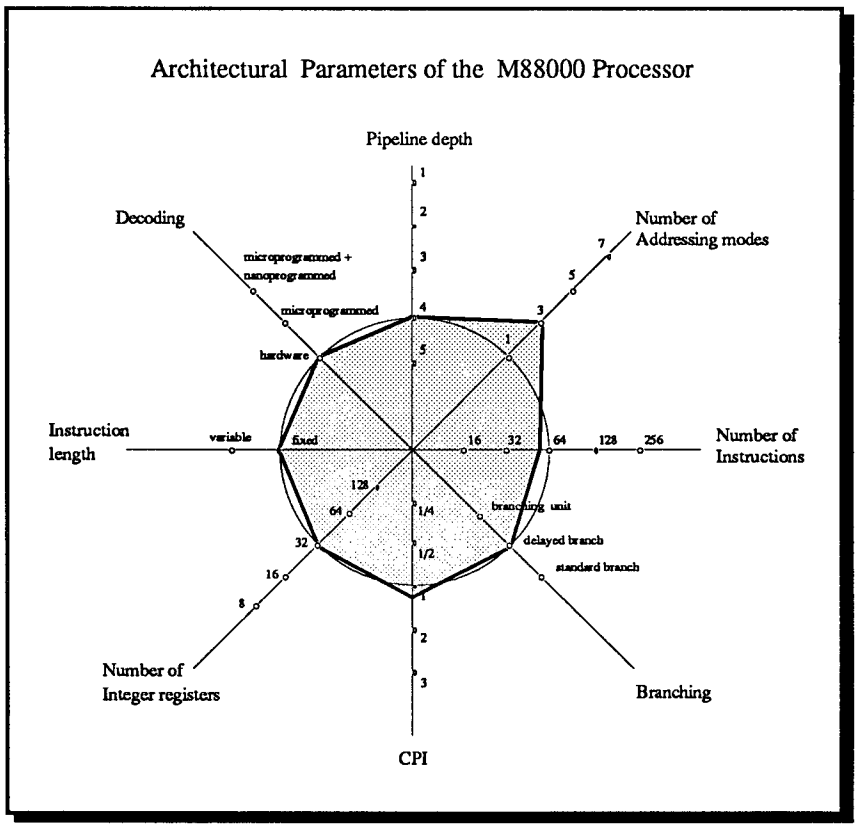

Figure 4

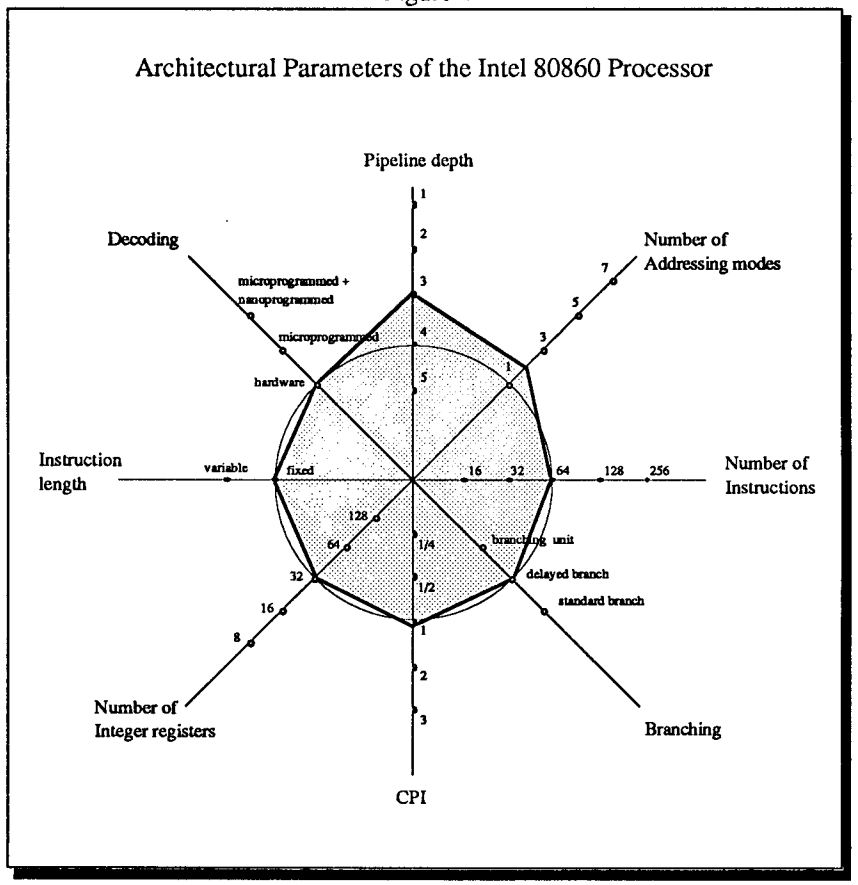

Figure 5

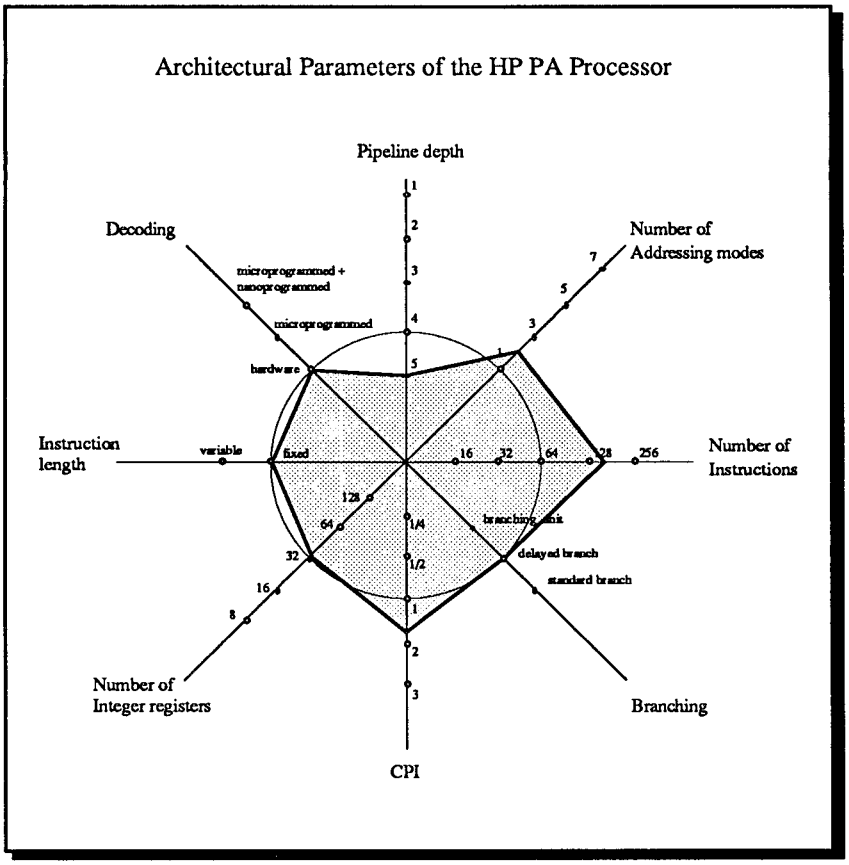

Figure 6

3. Comments

The six graphs shown before let us make some qualitative judgements about the processors involved. First of all, it is clear that every one of the processors considered approaches fairly good the ideal RISC circle. The MIPS R3000 processor is an example of a specially RISCy design. The SPARC falls apart of the other processors because of its large number of registers (used in conjunction with a special windowing technique). The IBM RS/6000 is a very complex design, with an instruction count well above typical RISC processors, with a special branching unit and more addressing modes as common. The M88000 and the i80860 look very similar (because in this comparison the floating point capabilities of each processor were not considered). The i80860 is the one with the lowest pipeline depth. The HP Precision Architecture is similar to the RS/6000 in its huge instruction count.

The graphical comparison shows considerable differences when we consider CISC designs. Figures 7 and 8 show the architectural parameters of the Transputer and the Motorola 68020. Both processors make use of similar technology and both are far away from the ideal RISC circle. It would be interesting to compare in this way some of the new CISC processors with a "RISC Kernel," like the 80486 or the 68040.

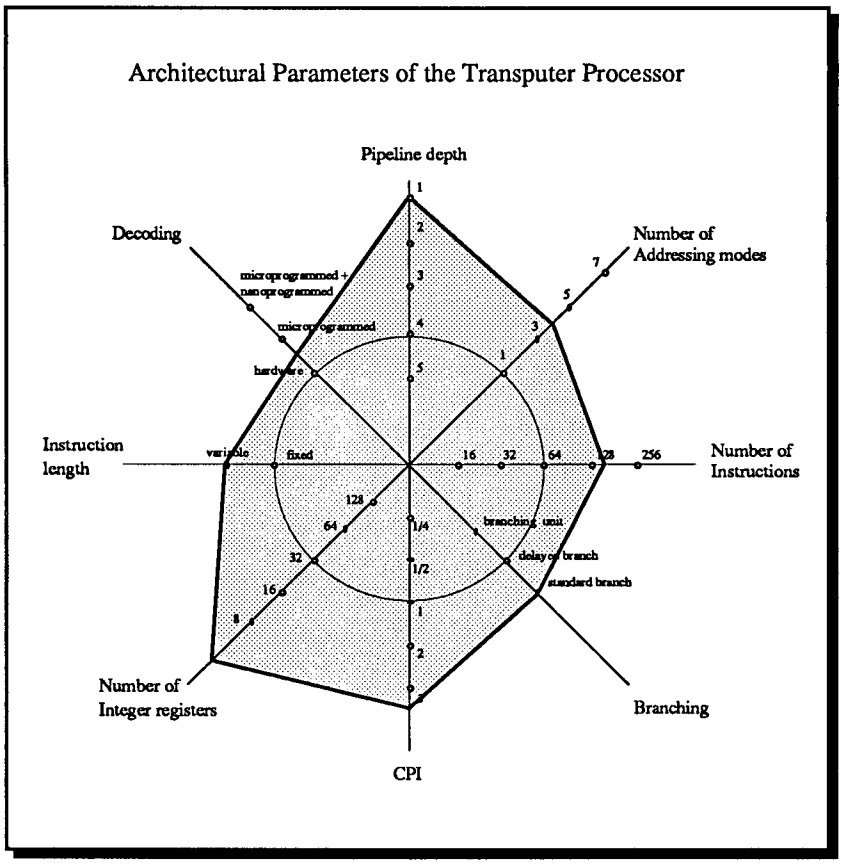

Figure 7

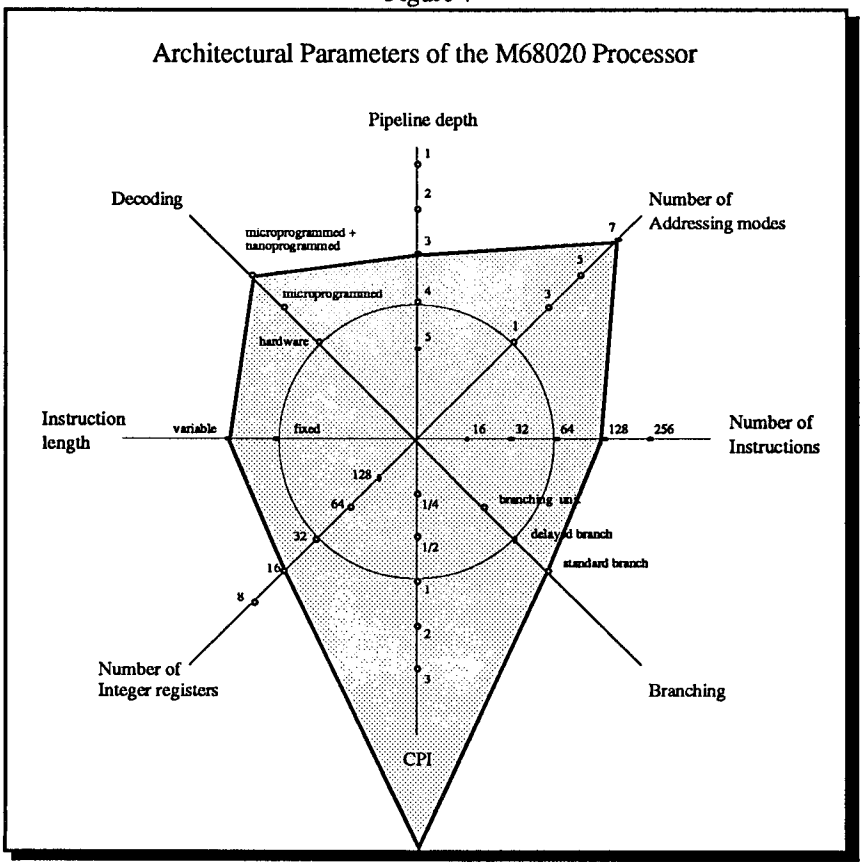

Figure 8

4. Epilogue

One picture says more than thousand words. We hope that the graphs shown can be used in the classroom to initiate stimulating discussions about the principles which lay behind the great success of the RISC concept in the marketplace. It would be interesting to look at the parameters of new RISC processors in this way when more information becomes widely available.

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